PhD Proposal

The *Meshotron*: a co-processor for 3D Digital-Waveguide Mesh modelling

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Introduction

Digital waveguide (DW) modelling is a finite difference time-domain (FDTD) numerical method of solving the wave equation, based on time and space discretisation. Excellent results have been achieved with this method, especially in sound synthesis and acoustic instrument simulation. The most efficient string and brass instrument synthesisers are currently based on 1-D DW models. Interconnecting 1-D models to form multi-dimensional DW meshes (DWM) is straightforward. For example, 2-D meshes are directly applicable to percussion instruments.

This method's popularity is due mainly to the following reasons:

- The algorithm is extremely simple and intuitive.
- In the 1-D case, it is much more efficient than any other *FDTD* formulations.
- Its accuracy can be arbitrarily improved by increasing mesh density (at the expense of computation time).
- DWM models can be easily interconnected with other linear systems, such as digital filters, which makes them very flexible.

The 3-D case is especially relevant in room acoustic simulation[1]. 3D DW meshes can theoretically provide accurate room impulse response (RIR) measurements, since all wave propagation phenomena (reflection, absorption, diffraction, interference, etc.) are automatically taken into account. The main difficulty lies on the computational size of the problem; obtaining the impulse response of an average-sized room may take hundreds of thousands of iterations on billions of nodes. The development of high-performance parallel computing architectures based on application-specific hardware (*ASH*) units is a promising approach, considering the simplicity of the DWM algorithm and previous studies on the subject. The following hypothesis is put forward:

> *"3D DWM acoustic models can be very efficiently parallelised through data partitioning on a network of specifically designed co-processors, allowing a dramatic reduction in RIR calculation time when compared to what is currently achievable on general-purpose computing platforms"*

[1] Vide http://www.aes.org.pt/Encontros/Encontro8-Lisboa/Apresentacoes/Guilherme/apea_2006.ppt

Objectives

The main objective is the development of a hardware prototype capable of implementing the 3D DWM algorithm on a small (cubic) block forming part of a large 3D room model. It must be equipped with communication ports for initial configuration (from a host computer) and data transfer between blocks. This entails the following tasks (non-exhaustive list):

- Familiarisation with the 3D DWM modelling technique.
- Software implementation of the 3D rectilinear and tetrahedral mesh models.
- Parallelisation on a workstation cluster (under MPI, for example).
- Block specification: topology (both the rectilinear and tetrahedral structures should be considered), dimensions, word-length, etc.
- Processor architecture design and optimisation for speed.
- Hardware simulation and testing.
- Performance evaluation (*benchmarking*).

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